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G.Alexeev
B.Baldin
D.Denisov
S.Hansen
V.Tokmenin

ON-CHAMBER ELECTRONICS FOR MUON IAROCCI MINI-DRIFT TUBES
(Technical Specification)

INTRODUCTION

This paper describes the design parameters for the electronics for EF muon chambers for the D0 upgrade. These chambers are constructed from Iarocci mini-drift tube assemblies. The topics covered in this note include: the specifications for a single channel of Amplifier - Discriminator (AD), a 32 channel Amplifier - Discriminator Board (ADB), the Low Voltage (LV) and High Voltage (HV) power supplies and the slow control system[1].

The total number of 8-wire tubes used in the system is about 6000 (48000 individual channels of readout electronics). The tubes, AD-channels and ADBs will be manufactured and tested at the Joint Institute for Nuclear Research (JINR, Dubna) and shipped to FNAL for final assembly and commissioning.

The parameters and design of the AD-channel and the ADB have been a matter of discussion both at Fermilab and Dubna between October 1995 and February 1996. The specification now presented is based on our present understanding of the performance of Iarocci mini-drift tube chambers. Changes to this specification arising from R&D or other sources of new information will be discussed and will be included in an updated version of this document by mutual agreement of the members of the D0 muon group.

1. AMPLIFIER - DISCRIMINATOR BOARD

The AD-channel consists of a wide band preamplifier and a fast discriminator with a variable threshold. The schematic diagram of the amplifier-discriminator is shown in Fig.1. An essential feature of the proposed design is the differential CMOS current driver at the output. This reduces parasitic feedback to the inputs in comparison to voltage mode drivers, thus increasing amplifier stability.

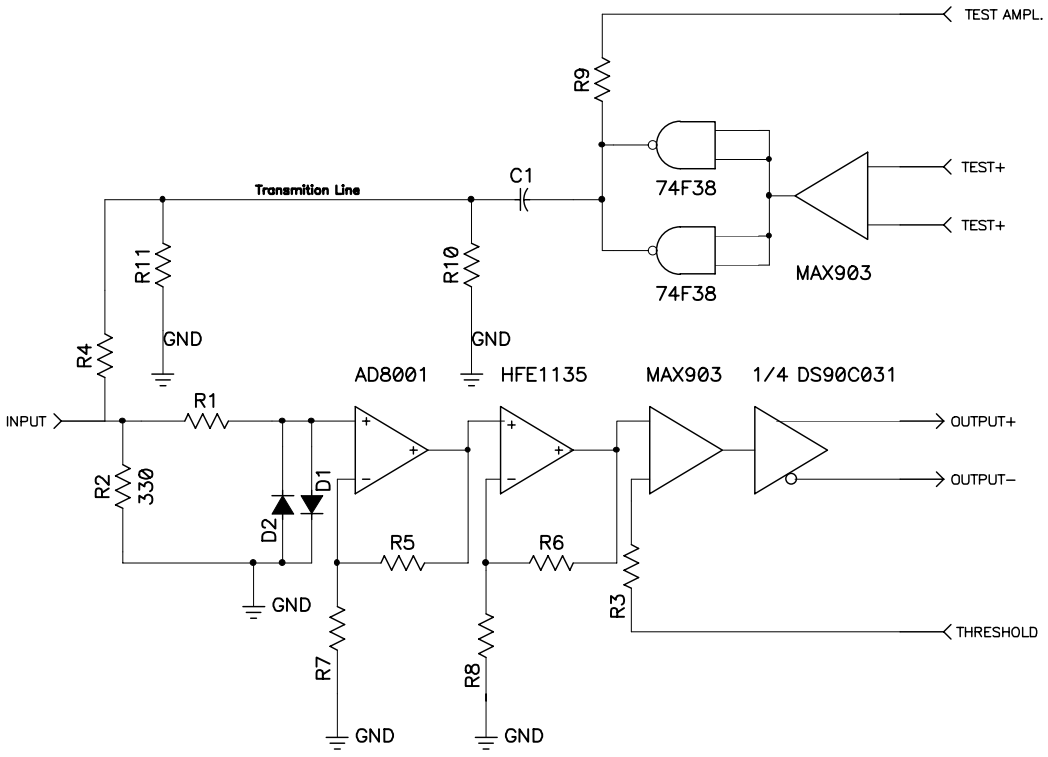

Fig.1 Amplifier–Discriminator channel

A test signal supplied by front-end electronics fires a local test pulser. The amplitude of the pulser is controlled by an analog voltage from the front-end electronics board. All the channels of one ADB are fired by the test signal simultaneously.

Two versions of the AD-channel design are proposed. The first version consists of two monolithic (solid-state) chips (an 8-channel preamplifier and an 8-channel discriminator). The second version is implemented in Surface Mount (SMD) technology. Both versions of the AD-channel are going through R&D at present, and one of the two will be chosen based on the outcome of a full scale mini-drift chamber prototype test.

The target specifications for an individual AD-channel are:

Amplifier gain (R load = 1 kOm)	- 100 /μA (2x50 mV/μA)
Noise (Cd = 0) at amplifier output	- 50..70 nA RMS Note 2
Rise time	- < 10 ns
Dynamic range	- 40..60 dB Note 2
Variable threshold range	- 0.5..5 μA
Output impedance	- high (current driver)
Output signal	- differential 4..5 mA
Power supplies	- ± 5 V

Notes: 1. The above specifications may have minor changes after completion of the R&D stage.
2. The worst case values occur for the SMD version and possibly will be improved in the monolithic version.

We propose that the granularity of the electronics should be 32-channels (one board for four eight-wire mini-drift tubes). Each channel can be inhibited at the input of the front-end digitizing card[/2/] located in a VME crate on the detector platform. Each 32 channel Amplifier Discriminator Board consists of the following parts:

- 32 channels of amplifier-discriminator
- input and output connectors
- DC voltage controlled test pulser with variable output
- low voltage filters
- low voltage fuses
- low voltage indicators (LED)

A 64 channel ADB version is under a consideration and the decision whether or not to use it will be made after this prototype is tested. The ADB should be located at a short distance from the end-plug of drift tubes. The worst case performance of the ADB can be no worse than:

- Noise	- 100 nA RMS
- Crosstalk between channels	- less than - 40 dB

The connection of the electronics to the tubes should be implemented using a short run of shielded wires. Complete RF shielding of the tubes is expected to be a part of mechanical design. For connection of the ADB's output to the front-end card in VME crate

we are planning to use 80-conductor high density cable (e.g. Amphenol Spectra-Zip PVC .025" Cable - 191-3003 Series) and corresponding connectors (e.g. 3M or Robinson Nugent). The length of these cables is defined by the location of the corresponding VME crates with respect to the on-chamber electronics. It is necessary to equalize the length of the cables within one front-end VME module (192 channels) in order to reduce the width of the gate signal within one front-end module. There is one gate signal per 192 channel module.

2. LOW VOLTAGE SUPPLY

We propose to use the power supplies currently installed in the muon system. As stated earlier, a bipolar ±5 V supply is needed for the on-chamber electronics. At a power consumption of about 100 mW/channel, the total power will be about 5 kW. If we assume that the muon chamber octants are equivalent, then 100 W power of LV per module is needed. For safe detector operation it is necessary to apply the following condition: the LV power cables should be able to withstand a short circuit in any part of the on-chamber electronics. Therefore it is necessary to take the following protective measures:

- implement fuses for each voltage
- power supplies must have over-voltage protection

To decrease the voltage drop on the power cables, the supplies have to be placed as close to the chamber modules as possible. To monitor the outputs of the LV supply, we propose to use the existing Monitor Board[/3/] .

3. HIGH VOLTAGE SUPPLY

We propose to use the 48 eight-channel HV modules currently installed in present muon system. The mini-drift tube HV supply must deliver up to 5 kV at 2 mA per channel. Each tube will have an individual connector to the HV bus. This allows us to disconnect an individual tube (8 channels) in case of any HV problems.

4. SLOW MONITORING

We propose to use the existing muon Monitor Boards(MB) to measure LV power supply voltage, current, chamber gas flow, pressure etc. Each MB has input and output registers, multiplexed ADC and DAC etc. This monitoring is necessary for the safe and reliable operation of the detector.

The list of parameters to be monitored includes:

- output voltages of LV supply
- gas flow through the chambers
- gas pressure
- temperature in a few points around EF muon system

Parameters of the HV power supply such as individual voltages and current limits will be controlled by the existing CDAQ system[4] .

5. READOUT ELECTRONICS TIMING

The timing scheme for the D0 muon system in RUN II is based on synchronization to the main Tevatron frequency of 53 MHz[5] and is shown in Fig.2. To define the timing of the readout electronics the following parameters must be considered:

- minimum bunch crossing interval - 132 ns
- maximum drift time - 60 ns
- maximum propagation delay along a 6 meter tube - 20 ns
- differences in arrival times for 192 channels in one octant - 5 ns

Based on the sum of all contributions to the difference between signal arrival time and bunch crossing, the gate width in VME front-end digitizing card should be not longer than 90 ns.

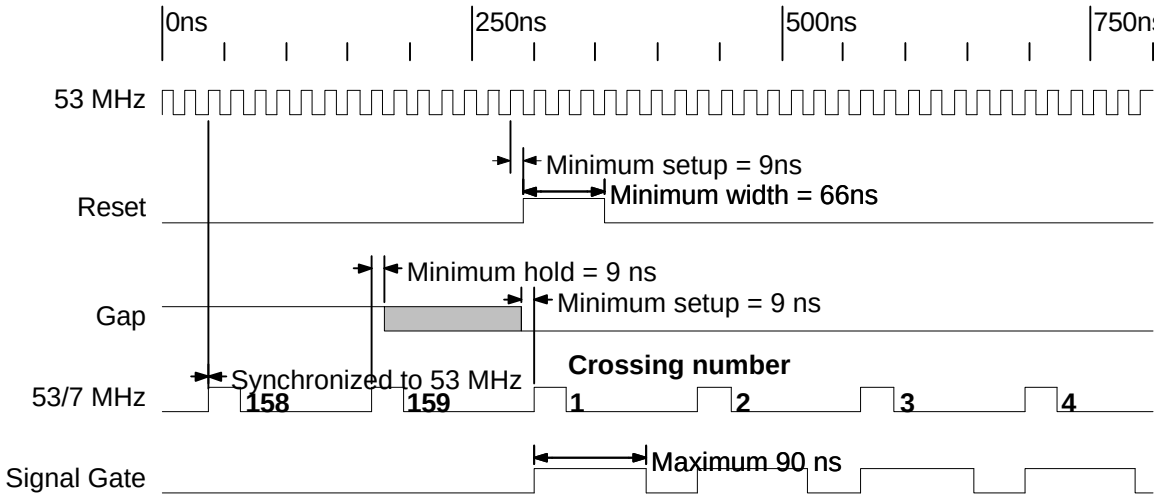

Fig.2. Mini-drift tube electronics timing diagram.

REFERENCES

1. R.Janyanti, K.Johns et al. The D0 Muon System Upgrade. D0 Note 2780, February 1996.
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4. R.Goodwin, R.Florian, M.Jonson at al. Initial operation and current status of the Fermilab D0 VME based hardware control and monitor system. NIM A293 (1990) pp. 125-129
5. B.Baldin, S.Hansen Proposed timing scheme for D0 detectors in RUN II. D0 Note 2708, 7/7/1995.